Evaluation of cluster support for nanotechnology – III-V MOSFET Nanoelectronics

Report to Scottish Enterprise Edinburgh and Lothian

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Contents

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1: Introduction

1.1 This is SQW Limited's report on an evaluation of a technology development and commercialisation initiative funded by the Scottish Enterprise (SE) Microelectronics & Opto-electronics Cluster Team (MOCT).

Background

1.2 Scottish Enterprise is providing £730k to the Electrical and Electronics Engineering Department at the University of Glasgow. The funding is for 3 years, between 2005-2008.

1.3 SE is funding two distinct projects associated with the University's research efforts directed towards III-V MOSFET technology. These projects are referred to in this document as:

- Circuit Design project, led by Professor David Cumming
- Scanning Capacitance Microscopy (SCM) project, led by Professor John Weaver.

1.4 Each is associated with the development of enabling technology relevant to the wider III-V MOSFET research programme led by Professor Iain Thayne.

1.5 As part of its work in support of key clusters, Scottish Enterprise took Professor Thayne and other academics on a tour of the USA during 2001-2. During this tour, the academics met with representatives of Sematech, the US-based consortium of major electronics companies which collaborates on pre-competitive research. One of the consortium members, Freescale (formerly past of Motorola), expressed special interest in the work at the University of Glasgow.

1.6 In 2004 Thayne received a £3m grant from the Engineering and Physical Sciences Research Council (EPSRC) for his research, plus £1.2m from the Scottish Higher Education Funding Council (now the Scottish Funding Council) for capital equipment. The EPSRC programme formally engaged Motorola (now Freescale) in Thayne's research. However, two parts of the EPSRC submission, on Circuit Design and SCM, were not supported.

1.7 We understand that in the light of this, and with Scottish Executive encouragement, SE decided to fund the two excluded "developmental" projects.

1.8 The initial EPSRC grant funding ended in 2006. The SE-funded development projects started in March, 2005 and run for 3 years. The SE funds support one PhD studentship on the Circuit Design project and two Research Assistant (RA) posts, one allocated to each of the two projects.

1.9 To ensure compliance with State Aid regulations and maintain appropriate levels of confidentiality, "Chinese Walls" were erected within the University between the EPSRC/Freescale programme and the two projects funded by SE.

1.10 In February, 2007 Thayne was awarded a further grant of £3.9m by EPSRC. This enables a re-integration of the various related R&D strands associated with the III-V MOSFET work.

Scope and purpose of the evaluation

1.11 The SE-funding initiative still has c.12 months to run and to this extent SQW's role has been to conduct an interim evaluation. We note that in the internal SE approval paper (dated November, 2004), there is an acknowledgment that some of the outcomes set for the initiative will take time to materialise, i.e. beyond the term of the present SE funding. As will be shown below, this is likely to be the case. (Indeed, once consultee doubted this was the right time for an evaluation – "too early to judge the commercial outcome and economic impact".)

1.12 The purpose of the evaluation primarily is to investigate the extent that the outcomes agreed for the initiative either have been realised or appropriate progress is being made towards their likely achievement. However, in addition to an explicit set of desired outcomes, we understand that the rationale for funding is associated with the achievement of wider strategic added value for the microelectronics and opto-electronics cluster in Scotland – to help develop and sustain strategic relationships with leading international companies and to develop a critical mass of excellence in R&D activity and capability in Scotland.

1.13 A key purpose behind the SE support was the wish to "back a good team" working in R&D relevant to a key industry for Scotland. There was also a concern that important Research Assistant (RA) capability would drift away from the Glasgow team without further support. Staff retention, and specifically experienced RAs, is rightly considered to be important to the maintenance of expert capability.

1.14 As is our practice, we place a strong emphasis in this evaluation report on the identification of "learning for development" issues.

Methodology

1.15 This evaluation involved a mix of desk and primary research conducted during February-March, 2007. Our desk research reviewed: the original SE approval paper; minutes of quarterly project management/monitoring meetings; development plans for each of the projects; promotional information on the two technologies under development.

1.16 Our primary research involved the following:

- face-to-face consultations with professors Thayne, Cumming and Weaver
- telephone interview with Lynne Brown, the member of staff within the University's commercialisation function with responsibilities for the two projects
- telephone interview with Neil Francis of Scottish Enterprise Edinburgh and Lothian.

1.17 We also received a full briefing on the projects and on the evaluation requirements from Mike Robertson of SE's MOCT at an inception meeting.

Structure of the evaluation report

1.18 The following report is structured as follows:

- Section 2 – examines achievements of and progress towards desired outcomes

- Section 3 – summarises key learning issues
- Section 4 – provides conclusions and recommendations.

2: Achievement of outcomes

2.1 In this section we provide evaluation evidence on the achievement of desired outcomes, or progress towards them.

2.2 The set of outcomes considered in Tables 2.1 to 2.4 is that described in Appendix 6 of the original SE approval paper. These outcomes are expected to be delivered by the University, albeit with support of SE's MOCT.

Table 2-1 Outcome category: elevated platform/improved visibility

Description	Set for Circuit Design project	Achievements/ progress	Set for SCM project	Achievements/ progress
PUBLICATIONS	In Years 2-3	Manuscripts in preparation for publication in 2007	In Years 2-3	Manuscripts in preparation for publication in 2007
CONFERENCES/ SHOWS	1 international per annum 1 UK per annum	Relevant events attended by team members although not yet to present papers.	1 international per annum 1 UK per annum	Relevant events attended by team members although not yet to present papers. Papers at 2 conferences planned: IEEE and ISTFA Testing and Measurement Conference.
NETWORKING ACTIVITY	Typically 2 meetings per annum	Researchers are in fairly dialogue with relevant businesses. Also engaged in UK-wide research collaboration.	Typically 2 meetings per annum	Researchers are in fairly regular dialogue with relevant businesses

Other comments:
Contacts with companies have led to valued letters of industry support when making bids for research funding.

Researchers are conscious of the importance of timing with respect to project progress in choosing time to present results at industry-relevant conferences.

Overall, these activity and output based "outcomes" are being met or likely to be met by end 2007.

Table 2-2 Outcome category: industrial collaborations

Description	Set for Circuit Design project	Achievements/ progress	Set for SCM project	Achievements/ progress
Meetings with companies	Tech transfer and commercialisation, follow-on project scoping	Researchers are in fairly dialogue with relevant businesses. See collaborative outcomes below.	Tech transfer and commercialisation, follow-on project scoping	Researchers are in fairly dialogue with relevant businesses. Strong interest in the SCM from Agilent: follow-on industry support anticipated
Student support	e.g. EPSRC CASE awards	Quinetiq and HMGCC CASE awards	e.g. EPSRC CASE awards	EPSRC funded award
Consultancy	Work for hire as appropriate	None directly associated with SE project to date	Interaction via KNT	None directly associated with SE project to date

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In-kind collaboration	Process libraries/data	To be progressed	Sample/device exchange	Prototype in advanced stage of development which will enable this.
Publicly funded projects	DTI, ECFP7, EPSRC	SE support assisted University win EPSRC support for Electronics Design Centre. The EDC has received c. £3.5m of financial support which has led to funding three new lectureships SFC has provided £600k through a SRIF award used to refurbish laboratory facilities. Also enabled participation in major UK collaborative e-Science Device Modelling research group.	DTI, ECFP7, EPSRC	Follow-on support of £4m recently awarded by EPSRC will fund MOSFET research that will specifically use the SCM capabilities.

Other comments:

It is the EPSRC-funded programme that has brought links with Freescale in the USA to date, not the two SE funded projects. No links with Freescale in East Kilbride. The University has a contract with Freescale and receives in-kind support, but via Thayne's research.

References to advances required in metrology in the ITSR "roadmap" are being addressed by the SCM project.

The development of collaborative links with US-based companies has been assisted by SDI. The wider MOSFET work has led to links with. Intel and IBM

Professor Cumming argues that the SE funding could claim greater than 20% of the credit for the success in winning EPSRC support for the EDC.

Professor Cumming has links with Freescale's international R&D function. Via EDC, he has links to Fujitsu and Quinetiq (the latter via an EPSRC CASE award) and to HM Government Communication Centre (also via a CASE award).

Arguably, the more significant and quantifiable outcome measures have been achieved, albeit attribution in some cases is shared with the wider III-V MOSFET capability within the University.

Table 2-3 Outcome category: training

Description	Set for Circuit Design project	Achievements/ progress	Set for SCM project	Achievements/ progress
Undergraduate sponsorship	Via departmental teaching programmes	The winning of EDC funding, helped by SE support, has led to new lectureship appointments.	Via departmental teaching programmes	No specific sponsorship outcome.
PhD sponsorship	Fully funded or CASE	Quinetiq and HMGCC CASE awards	Fully funded or CASE	New EPSRC funding of £4m for MOSFET work has included funds for a PhD project.
EngD support	In partnership with ISLI	No involvement of ISLI to date. Originally thought that it might take forward the work on Circuit Design.	- - -	
Research assistantships	Support industry via post-doc contracts	SE funding proved crucial in supporting an RA post working on technology development of interest to industry.	Support industry via post-doc contracts	SE funding proved crucial in supporting an RA post working on technology development of interest to industry.

Other comments:

Since SE's funding, the University's design activity has been enhanced. The SE funding allowed the University to demonstrate prior funding for Circuit Design work and to obtain letters of support. It also allowed the University to demonstrate strategic commitment to this area of work. All of this helped secure funding from EPSRC and SFC for the Electronics Design Centre.

The outcomes concerned with CASE awards and RA support have been achieved. The ISLI involvement appears unlikely.

Table 2-4 Outcome category: ownership

Description	Set for Circuit Design project	Achievements/ progress	Set for SCM project	Achievements/ progress
Know-how	Technology transfer	The interest by industry in the projects implies relevant know-how development.	Technology transfer	The interest by industry in the projects implies relevant know-how development.
Patents/IP	At least one	Building blocks for an IP position are being created. Patent review under way.	At least one	Protectable designs in University ownership.
Licensing	At least one	Not yet. Further development work after SE funding term required. License route anticipated.	At least one	Not yet although recent breakthrough has been made. Expected to be licensable over next 2-3 years.

Other comments:
In the SCM project, work on the development of a prototype that can be used as a demonstrator with companies is well advanced.

Challenge for both projects now is to find funding for more development work before licensing or other form of commercialisation will be possible.

UoG's background IP position is now much stronger than it was at the outset of the EPSRC/Freescale programme and thus more accessible.

On SCM project, the University has a strong ownership position with respect to background IP now relevant when in discussion with Agilent.

On SCM project, needs further developmental work until end of SE funding, end of year, then technology should be ready to work on commercialisation. Professor Weaver is keen to be able to deliver "hard numbers" as outputs before approaching potential licensees.

The licensing outcome has yet to be achieved – this is to be expected given than the technology development process is still underway - and the formal protection of IP is under review rather than yet achieved.

Summary or outcomes

2.18 A substantial number of the "outcomes" have been achieved, notable those related to third party funding and industry links. However, in some cases at least attribution to the specific SE funding input is shared, not surprisingly, with the deeper and longer standing MOSFET research capability within the University.

2.19 The commercialisation outcomes have not yet been achieved. It would probably be surprising if they had been by now. It will be important for SE to ensure that existing momentum is maintained after its funding ends.

2.20 The SCM project appears to offer the prospect of transfer to industry within the short to medium term. The time frame for transfer of the Circuit Design work appears to be more problematic.

3: Strategic issues arising

3.1 The exclusion of the two SE-funded projects from the initial EPSRC award does not appear to have come as a surprise to some consultees. As well as describing them as "developmental", it is acknowledged that the University did not have at the time the appropriate metrology capabilities nor the transistor technology capabilities that were required. The SE funding has rectified these deficits.

3.2 When asked about the criticality of SE funding, consultees indicate that if it had not been forthcoming it would: "not have been make or break for the University's MOSFET research efforts" – SE's funding was "very positive, but not critical". However, whilst other routes to funding may have been available, this may have delayed advances and resulted in the loss of key team members.

3.3 Whilst the SCM project specifically may have been able to find funds from other sources, at the time the University did not have a track record in the subject area and thus any proposal would have been hard to sell. It would almost certainly have led to delays in getting the work started. Having had the SE support, the University is now much better prepared to seek funds for metrology work from other sources.

3.4 As a result of SE support, metrology has been now embedded within the work funded by the new EPSRC award. The SE-funded Circuit Design project contributed to the case for funding of the Electronics Design Centre (EDC). The latter award helped in gaining recognition, including in Scotland, for the University's III-V MOSFET activity.

Sustaining teams

3.5 One consultee pointed to the problems which arise from the gaps in time between EPSRC funding opportunities. This impacts the ability to retain key staff in the research group, notably RAs. Bridging funds to retain RAs is a key requirement. The SE funding has proved critical in sustaining research teams, especially RAs.

Relevance of other SE-backed funding sources

Role of the ITI Techmedia

3.6 We were informed that the relevant Intermediary Technology Institute (ITI Tech Media) had shown little interest in the work to date as potential commercial returns were seen to be too far in the future, perhaps up to 10 years away – "the ITI is not interested in investing in speculative projects". One consultee argued that the developmental work funded by SE could, however, realise a commercial value much earlier.

3.7 We understand that the ITI was interested at outset, is willing to assist, but nothing has been done to date. We suggest that the ITI could assist with providing useful market signals to the University from its market scanning/foresighting, especially for the Circuit Design project.

3.8 We are advised that Circuit Design development could be integrated into major design tools internationally and should be of interest to an ITI. It could be of interest to a company such as Cadence. It may be 8-10 years way from the mainstream market, but perhaps only 3-5 years ways from use in Radio Frequency tools. The market for the SCM may prove too small for ITI interest.

3.9 However, one consultee argues that because of the way the ITI works one cannot go to it with a proposition, but rather must wait to respond to a tender.

Proof of Concept Fund

3.10 The Proof of Concept funding is seen as not appropriate to these projects up until now: it is perceived as being too focused on projects with spin-out potential. Also it is for too short a funding term.

3.11 We understand that Professor Weaver has submitted a PoC bid to conduct work similar to the SCM project now being funded by SE but it was rejected as the market for the technology was seen as too narrow to be attractive. The PoC reviewers expected the commercial returns to be too small.

3.12 One academic consultee acknowledges it would have been premature to expect PoC funds for these projects until now – "maybe ready now".

Timing of support

3.13 A key issue for SE now is what happens next. Having supported "developmental" projects, but ones which still require further time and support to achieve the subset of outcomes that relate to commercialisation, does it stay engaged by exploiting the flexibility of its funding instruments or now leave the projects to the "fate" of its own competitive funding streams or to the market?

3.14 This dilemma is almost inherent when an economic development agency intervenes in this kind of way and at this stage in technology development, with a mix of wider and longer term strategic added value and more direct commercialisation- related outcome targets. It is not clear how the support for the route to market, if public sector support is indeed still required, will now operate.

4: Learning for development issues

4.1 Our consultees pointed to a number of specific process lessons based on the operation of the SE funding. These are:

- the role of the SE project manager has proved to be highly valued and effective
- administrative demands placed by SE have proved to be quite onerous
- one academic consultee is disappointed that SE has not made the level of quality links with businesses in the UK/Scotland that it seemed to promise
- flexibility over SE budget transfer between quarters would be helpful – projects of this kind involve technical risk that impacts spend schedules
- the "Chinese Walls" between the SE projects and the original EPSRC/Freescale work has been problematic in terms of communication at times, but overall it has not adversely affected the SE projects
- being unable to recruit staff on SE funding unless dedicated to the SE project presents problems
- SE not funding overheads also presents problems
- quarterly project meetings have been burdensome, but overall it is acknowledged that they have added value.

5: Conclusions and recommendations

5.1 Overall, the outcomes wanted from the SE funding of the two development projects have either been achieved or reasonably expected. The achievement of licensing outcomes is of course surrounded by market-related uncertainties. However, through both projects and more widely through Professor's Thayne's MOSFET research, the University is establishing and maintaining links with important international companies that can only make it more likely that commercialisation outcomes will be achieved.

5.2 Following SE support, the University has been successful in winning additional funds both from EPSRC and on a smaller scale from industry. Notably, attribution to SE at level of greater than 20% is offered by an academic consultee in the success of winning £3.5m from EPSRC for the Electronics Design Centre – in crude terms almost a match for the SE investment.

5.3 Other leverage has undoubtedly been obtained but in reality the success in winning additional funds and in enhancing links with industry have a shared attribution, to SE's funding and to the excellence and reputation of the University's wider research capabilities in MOSFET technology.

5.4 It will, however, be important to sustain momentum once the SE funding ends. There is a need for SE to determine the kind of role it will play in this ongoing process.

5.5 For the Circuit Design project in particular, we recommend that SE explores with the ITI Tech Media whether it can assist the University in tracking market signals in terms of the likely take up of the relevant technology internationally.

5.6 The flexibility and responsiveness of SE in funding these two projects is clearly welcomed by the researchers involved. SE approval for the intervention was built on a mix of desired outcomes – "visibility", "industrial collaborations", "training" and "ownership" of IP. Other objectives around building critical mass play into the mix. For the University, however, one of the key outcomes relates to establishing and sustaining high quality research teams within an internationally competitive environment, in particular bridging between Research Council funding rounds.

5.7 Arguably, the SE funding in this instance has either deliberately or by chance of timing helped to "treat" the problem of sustaining research teams, but it is not offering a "cure". We recommend that a deeper investigation, perhaps in conjunction with the Scottish Funding Council, is required into the true extent of the "problem" of sustaining key, strategically important research teams and if appropriate a more direct intervention considered.